CLAIMS:

1. A module for transmitting (52) a plurality of data bits (d0,d1,d2,d3) to another module (56) via a communication bus (54), the module (52) comprising:

- means adapted to generate respective copies (c0,c1,c2,c3) of the data bits;
- means (520,521,522,523) adapted to invert the respective copies of the data bits; and
- means adapted to transmit, via the communication bus (54), the plurality of data bits and their respective inverted copies (c0',c1',c2',c3') to the other module (56).

2. A module (52) as claimed in claim 1, further comprising:

- means (58) adapted to generate a first parity bit (Tparity) from the plurality of data bits (d0,d1,d2,d3);

wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits (d0,d1,d2,d3) and their respective inverted copies (c0',c1',c2',c3'), the first parity bit (Tparity) to the other module (56).

3. A module (52) as claimed in claim 2, wherein the means (58) adapted to generate a first parity bit comprises one or more logic gates (60,62,64).

4. A module (52) as claimed in claim 2 or 3, further comprising:

- means (520,521,522,523) adapted to generate an inverted copy of the first parity bit (Tparity);

wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits (d0,d1,d2,d3), their respective inverted copies (c0',c1',c2',c3') and the first parity bit (Tparity), the inverted copy of the first parity bit (Tparity') to the other module (56).

5. A module (56) for receiving a plurality of data bits (D0,D1,D2,D3) from another module (52) via a communication bus (54), the module (56) comprising:

- means adapted to receive the plurality of data bits (D0,D1,D2,D3) and respective inverted copies (C0',C1',C2',C3') of the data bits from the other module (52);

- means (68) adapted to detect the presence of one or more errors in the received data bits (D0,D1,D2,D3);
- means (Mux0,Mux1,Mux2,Mux3) adapted to select the received data bits (D0,D1,D2,D3) as the output of the module (56) in the event that the means (68) adapted to detect the presence of one or more errors does not detect any errors, and to select the inverse of the respective inverted copies (C0',C1',C2',C3') of the data bits as the output of the module (56) in the event that the means (68) adapted to detect detects the presence of one or more errors.

6. A module (56) as claimed in claim 5, wherein the means adapted to receive is further adapted to receive a first parity bit (Tparity) from the other module (52); and wherein the module (56) further comprises:
- means (66) adapted to generate a second parity bit (Rparity) from the received data bits; and
wherein the means (68) adapted to detect the presence of one or more errors in the received data bits is adapted to compare the first and second parity bits.

7. A module (56) as claimed in claim 6, wherein the means (68) adapted to generate a second parity bit (Rparity) comprises one or more logic gates.

8. A module as claimed in 6 or 7, wherein the means (68) adapted to detect the presence of one or more errors in the received data bits comprises a logic gate.

9. A module (56) as claimed in claim 5, 6, 7 or 8, wherein the means (Mux0,Mux1,Mux2,Mux3) adapted to select comprises one or more multiplexers, each multiplexer having a received data bit and the inverse of its respective inverted copy as inputs, and wherein each multiplexer is operable in response to a control signal (s0) output by the means (68) adapted to detect.

10. A module (56) as claimed in claim 5, 6, 7 or 8, wherein the means (Mux0,Mux1,Mux2,Mux3) adapted to select comprises one or more multiplexers, each multiplexer having the inverse of a received data bit and its respective inverted copy as inputs, and wherein each multiplexer is operable in response to a control signal (s0) output by

the means (68) adapted to detect, and wherein the output of the module (56) is the inverse of the output of each multiplexer.

11. A system comprising a module for transmitting (52) as claimed in one of claims 1 to 4 and a module for receiving (56) as claimed in one of claims 5 to 10, the modules being connected via a communication bus (54).

12. A method of reducing ground bounce in a system in which a plurality of data bits are to be transmitted from a first module to a second module via a communication bus, the system being able to detect errors in the transmitted data bits, the method comprising:

- generating respective copies of the data bits to be transmitted (step 1002);
- inverting the respective copies of the data bits (step 1004); and
- transmitting, via the communication bus, the plurality of data bits and their respective inverted copies to the second module (step 1006).

13. A method as claimed in claim 12, the method further comprising:

- receiving, via the communication bus, the plurality of data bits and their respective inverted copies from the first module;
- detecting the presence of one or more errors in the received data bits;
- using the received data bits as the output of the second module in the event that one or more errors are not detected in the received data bits;
- using the respective copies of the data bits as the output of the second module in the event that one or more errors are detected in the received data bits.

14. A method as claimed in claim 12 or 13, the method further comprising:

- generating a first parity bit from the plurality of data bits to be transmitted; and
- transmitting the first parity bit to the second module with the plurality of data bits and their respective inverted copies.

15. A method as claimed in claim 14, the method further comprising:

- receiving, via the communication bus, the first parity bit from the first module;
- generating a second parity bit from the received data bits;
- wherein the step of detecting one or more errors in the received data bits comprises comparing the first and second parity bits.

16. A method as claimed in claim 14 or 15, the method further comprising:

- generating an inverted copy of the first parity bit; and
- transmitting the inverted copy of the first parity bit to the second module with the plurality of data bits, their respective inverted copies and the first parity bit.